REMARKS

Applicants have cancelled claims 1-3, amended claim 4 to appear in independent form and to improve English usage, and added new claims 14 and 15 to cover the original scope of claim 4 that was multiple dependent. Applicants have also amended claim 5 to improve English usage. As a result, claim 4 and claims 5, 14 and 15 which are dependent from claim 4, when they issue, will not have been amended to bring them into compliance with any statutory requirement for patentability, and the full scope of equivalents will be available without prosecution history estoppel.

Claim 4 has been rejected under 35 USC 102(b) as being anticipated by U.S. Patent No. 5,936,265 (Koga). This rejection is respectfully traversed.

Claim 4 as amended recites a pair of electrode pad layers of the second conductivity type formed at both ends of the resistance layer of the second conductivity type. In his rejection of claim 4, the Examiner has not considered this limitation at all. Although Koga' s device has a pair of electrode pad layers 701, 702, one pad layer 701 of the pair is a P type layer and another pad layer 702 of the pair is an N type layer. See column 17, lines 57-61 and FIG. 23A, of Koga. On the contrary, the two electrode pad layers of claim 4 are layers of the same conductivity type, which is also the conductivity type of the resistance layer of claim 4. This distinction is significant because Koga's device is a surface tunneling effect element, or a diode (column 17, lines 49-52, of Koga), which requires two electrode pad layers of different conductivity types by nature, and the device of claim 4 is a resistor element, which must have the two electrode pad layers of the same conductivity for it to operate in a semiconductor device.

Thus, Koga does not teach or suggest the pair of electrode pad layers of claim 4. Accordingly, the rejection of claim 4 should be withdrawn.

Claim 4 has been rejected under 35 USC 102(b) as being anticipated by U.S. Patent No. 5,686,754 (Choi). This rejection is respectfully traversed.

Claim 4 as amended recites a pair of electrode pad layers of a second conductivity type formed at both ends of the resistance layer of the second conductivity type. In the resistor element of claim 4, the two electrode pads and the resistance layer are of the same conductivity type, i.e., the second conductivity type. This is a requirement for a resistor element to operate in a semiconductor device. On the other hand, Choi's device has two electrode pad layers 60, 61 of an N type, which are formed at both ends of a resistance layer 64. A polysilicon ring 71 and a corresponding electrode 71a, which the Examiner cited as the resistance bias electrode layer of claim 4, are positioned above the resistance layer 64. The resistance layer 64 of Choi is, however, a P type. Accordingly, the conductivity type of two electrode pad layers are different from the conductivity type of the resistance layer. This is because Choi's device is a MOS-FET, which requires the channel layer 64 to be of a conductivity type different from the conductivity type of the contact regions 60, 61. See column 3, lines 20-29 and FIG. 2, of Choi.

Thus, Choi does not teach or suggest the pair of electrode pad layers of claim 4. Accordingly, the rejection of claim 4 should be withdrawn.

Claim 5 has been rejected under 35 USC 103(a) as being unpatentable over Choi. This rejection should be withdrawn because Choi does not provide the teachings for which it is cited.

In light of the above, a Notice of Allowance is solicited.

Attached hereto is a marked-up version of the changes made to the claims by this amendment, captioned "**Version with markings to show changes made**".

In the event that the transmittal letter is separated from this document and the Patent and Trademark Office determines that an extension and/or other relief is required, applicants petition for any required relief including extensions of time and authorize the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 03-1952**, referencing Docket No. **492322002200**.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

4. (Amended) [The] A semiconductor device, [of claim 1, 2 or 3, further] comprising:

a semiconductor substrate of a first conductivity type;

a resistance layer of a second conductivity type formed on the semiconductor substrate, one end of said resistance layer being adapted to have a first voltage applied thereto, another end of said resistance layer being adapted to have a second voltage applied thereto;

an oxide film formed on the resistance layer;

a resistance bias electrode layer comprising a silicon layer formed on the oxide film; and

a pair of electrode pad layers of the second conductivity type formed at both ends of the resistance layer of the second conductivity type,

wherein the first and second [voltage is] voltages are applied to the corresponding electrode pad layers to provide the resistance layer with an electric current, and

the device is configured so that voltage dependence of a resistance of the resistance layer is reduced by adjusting the first and second voltages applied to the resistance bias electrode layer.

5. (Amended) The semiconductor device of claim 4, wherein the ratio of the voltage difference between the first and second voltages applied to the pair of the electrode pad layers to the voltage applied to the resistance bias layer is 0.5-0.6.

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